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Low Power, Asynchronous Multiplier

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***Abstract*— this paper presents an asynchronous multiplier. It uses the same multiplier model to establish the superiority of asynchronous circuits over synchronous circuits. The paper shows that asynchronous circuits are more power efficient than the conventional synchronous circuits. This paper takes the help VHDL models of synchronous and asynchronous multiplier circuits to establish the superiority of asynchronous circuits over their synchronous counterparts. The VHDL models are used for comparing the power performances of the two circuits.**

***Keywords*— Asynchronous Circuit, High Speed, Low Power, Synchronous Circuit, VHDL**

I. INTRODUCTION

Our computing devices are becoming faster and more robust than ever before. The evolution of these machines is so rapid that technologies, which were considered as breakthroughs and reserved only for scientific use about 5 years ago, are today commonplace. Such is the rapid growth in computer hardware that systems which were commonplace 10 years ago are considered obsolete today.

Our electronic systems today are predominantly based on synchronous designs having a global clock. These synchronous systems consume a lot of power even in the idle state when they are not processing any data. This stems out of the fact that they are attached to the global system clock. Power consumption, in an electronic system, is mainly related to signal transitions and stems from the charging and discharging of the parasitic capacitances in transistors and wires. Minimizing power consumption is, therefore, a question of avoiding unnecessary signal transitions. The system clock, in synchronous systems, is a source of electrical signal transitions and, thus, is a major factor while calculating the overall power consumption.

Asynchronous systems can provide a solution to this problem of high power consumption in synchronous systems. Asynchronous systems, contrary to synchronous systems, do not have a global clock. In such systems, the local clock of a specific combinational component activates only when that component is processing data. Hence the deactivation of the clock during idling leads to further power conservation.

This power saving may not be appreciable in everyday computing devices like personal computers but is extremely beneficial for systems which have limited battery power. For example, the satellites orbiting our earth derive their power from the sun. When these satellites travel through the shadow of the earth or through the shadow arising due to an eclipse, the solar panels of these satellites do not receive sufficient solar energy and thus are not able to generate enough power for the satellite to function. In such situations, satellites are put into power saving mode by temporarily shutting down some functions of the satellite. [4] These satellites can be made more resistant to such spells of power deficiency by using asynchronous systems to construct them. The satellites, then, would be able to fully function for longer periods during transitions through the shadow regions.

For the purpose of establishing the superiority of asynchronous systems over synchronous systems, the synchronous and asynchronous versions of a multiplier circuit have been designed using VHDL.

II. HANDSHAKING

The components of an asynchronous system interact with each other using request and acknowledge signals. This exchange of request and acknowledge signals is called handshaking. Two interacting components in a system are shown in Figure 1.

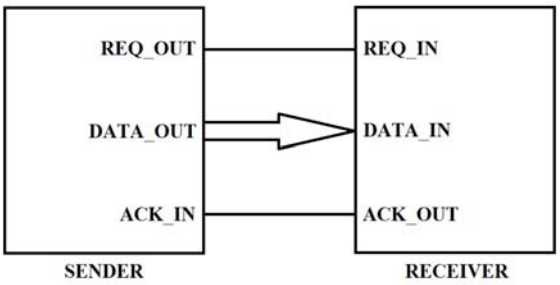

Fig. 1 Handshaking

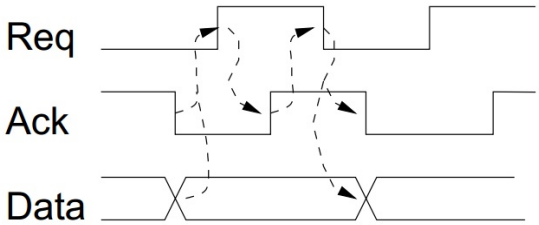

Fig. 2 Handshaking signal waveforms

A simple handshaking protocol may be implemented in the following way: (1) The sender issues data and sets request signal to high, (2) the receiver gets the data and sets acknowledge signal to high, (3) the sender responds to the high acknowledge signal by setting the request signal to low, (4) the receiver acknowledges this by setting acknowledge signal to low. At this point, the sender may issue the next data to be transferred. This is called the 4-phase protocol. Signal transitions which correspond to the 4-phase protocol are shown in Figure 2. Further description of the handshaking protocols can be found in [1] and [2].

III. VHDL Model Description

This paper uses VHDL models of synchronous and asynchronous multipliers. The multipliers take two 2-bit binary numbers as inputs and display their products as 4-bit binary numbers. All VHDL models presented in this paper have been created and synthesized by using Xilinx ISE, version 9.1i. The modelling has been done using CoolRunner2 CPLDs.

A. Synchronous model

The VHDL model of the synchronous multiplier contains the following ports – CLK, A (1:0), B (1:0), and PRODUCT (3:0). The ports have their usual meanings. The block diagram for the synchronous VHDL model is shown in Figure 3. Its NGR is shown in Figure 4.

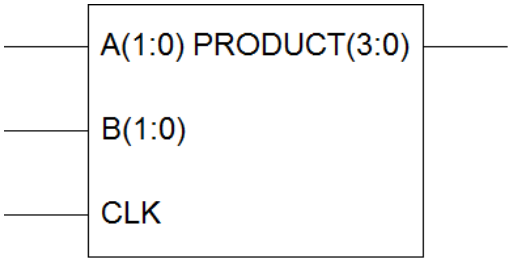

Fig. 3 Synchronous multiplier block diagram

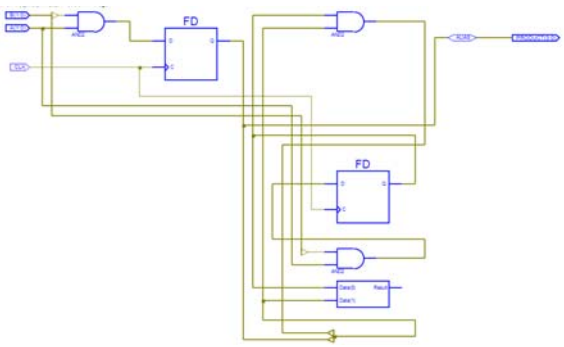

Fig. 4 Synchronous multiplier NGR

B. Asynchronous model

The VHDL model of the asynchronous multiplier contains the following ports – REQ (Request), A (1:0), B (1:0), PRODUCT (3:0) and ACK (Acknowledge). The ports have their usual meanings. The block diagram for the asynchronous VHDL model is shown in Figure 5. Its NGR is shown in Figure 6.

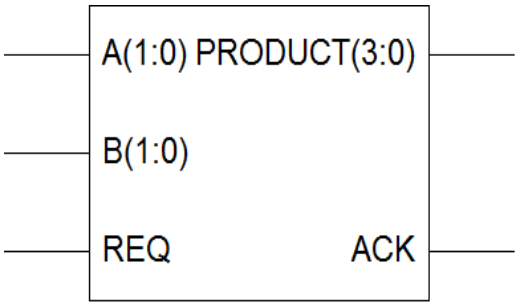

Fig. 5 Asynchronous multiplier block diagram

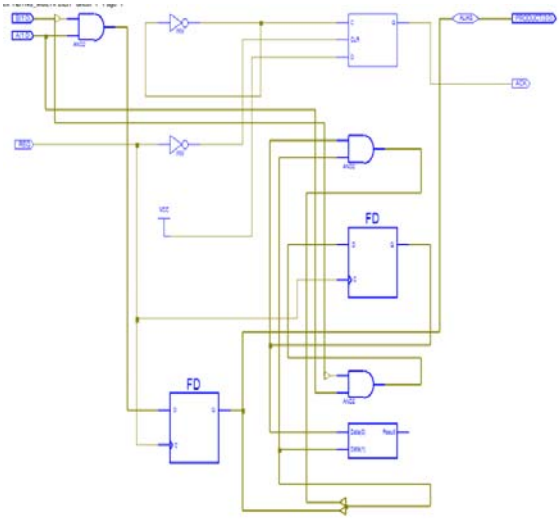

Fig. 6 Asynchronous multiplier NGR

IV. Analysis

The VHDL models for the synchronous and asynchronous multipliers have been created to analyze and compare the power characteristics of the two multiplier variants. The two VHDL models have been created using similar programming styles so that they relate to each other as much as possible. The power analysis, of the two multiplier variants, has been done using the xPower Analyzer tool which is bundled with Xilinx ISE. The test benches created for analyzing the power characteristics of the two variants were run for a time of 1000ns. A maximum of 4 operations could potentially be performed within this simulation time.

Test benches were created to replicate situations in which 1, 2 and 3 multiply operations are performed by the two multiplier models in the given simulation time of 1000ns. These test benches were then used to generate power reports for the two VHDL models. The data so generated is presented in Table 1 and Table 2.

From the tables, it can be seen that asynchronous circuits do provide an advantage over synchronous circuits in terms of power consumption. This advantage is maintained till a certain number of operations are performed per unit time. After that limit is reached, the asynchronous circuits consume more power than their synchronous counterparts due to the additional power consumed in carrying out handshaking by two interacting modules. Thus, modeling of system components, which are only used intermittently, as asynchronous components, can potentially result in large power saving. Taking this approach will enable our battery powered devices to work for longer periods between two recharges.

TABLE I
Power consumption in synchronous multiplier

Number of Operations	Dynamic Power (mW)	Quiescent (mW)	Total (mW)
One	0.409	0.029	0.438
Two	0.491	0.029	0.52
Three	0.791	0.029	0.82

TABLE III
Power consumption in asynchronous multiplier

Number of Operations	Dynamic Power (mW)	Quiescent (mW)	Total (mW)
One	0.385	0.029	0.414
Two	0.478	0.029	0.507
Three	0.781	0.029	0.81

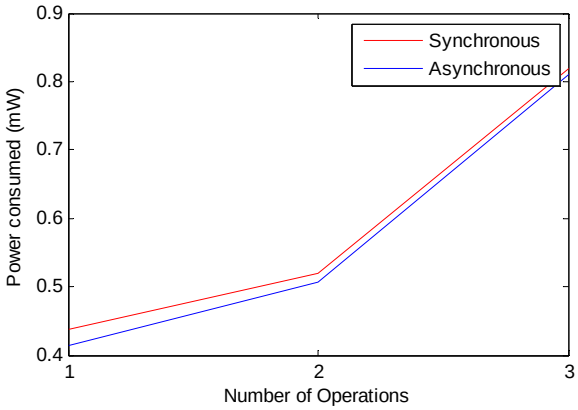

Fig 7: Power consumption comparison

V. Conclusion

The analysis of asynchronous devices in this paper shows that the asynchronous devices are more power efficient. This is due to the fact that asynchronous devices only consume power when they are activated by the request inputs unlike the synchronous systems which function continuously due to the continuous supply of clock signal. Thus, asynchronous circuits, with their advantage of low power consumption over synchronous circuits, have the potential to fulfill our needs for powerful computing machines.

References

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